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New LDMOS Model Delivers Powerful Transistor Library—*Part 1: The CMC Model*

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This new LDMOS model accurately predicts both small-signal and nonlinear performance, and is scalable for devices of different sizes and power output capabilities

A new LDMOS transistor model has been developed as a collaboration between W.R. Curtice Consulting, Modelithics and Cree Microwave. This article, the first of a two-part series, describes the background and development of the model. The model has been shown to scale well and fit signal, power and distortion performance for a wide range of device sizes.

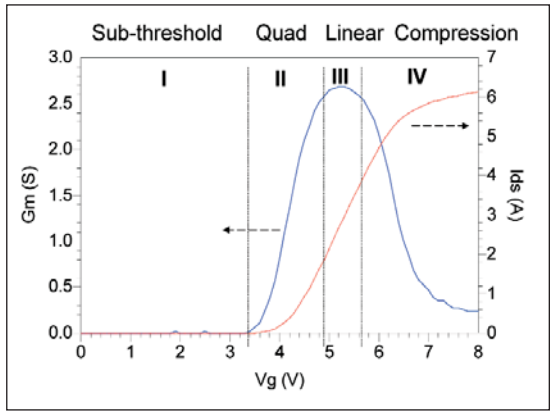

Figure 1 · Four region current behavior of the 1 watt LDMOS cell device used in this development.

Introduction

Non-linear transistor models are being increasingly utilized and demanded by the power amplifier design community because they provide access to multiple simulator capabilities, including DC analysis, as well as analyses of small-signal, nonlinear, time domain, and complex modulation effects. The availability of accurate, validated models eliminates the need for designers to make their own source and load pull and S-parameter measurements on every device, and allow fast "what-if" analysis e.g. change frequency band, drain voltage etc. Savvy semiconductor marketing departments are also recognizing that more and more design engineers use simulators to minimize design risk, reduce design spins and cut design time. Good models will ultimately sell more product.

It is well recognized that excellent power performance and linearity can be achieved at low cost using laterally diffused metal-oxide-semiconductor (LDMOS) transistors. In fact they are the technology of choice for base station applications below a couple of GHz as well as many other RF and microwave applications. Existing LDMOS FET large-signal models show a number of disadvantages. They tend to show poor prediction of IMDs, do not work in the sub-threshold region, lack a dynamic self-heating effect, do not use closed-form analytic equations to represent channel current, have complex extraction routines and do not scale well with the number of cells. Balancing the trade-off between linearity and efficiency and designing optimal matching and bias networks requires more accurate LDMOS models with better treatment of these effects. Moreover, increasingly complex digital modulation schemes are placing increased demands on model fidelity through 5th or 7th order distortion predictions.

This paper describes a new model that meets this challenge in an elegant and robust way. Part 1 of this paper outlines the topology and methods used to extract and validate a

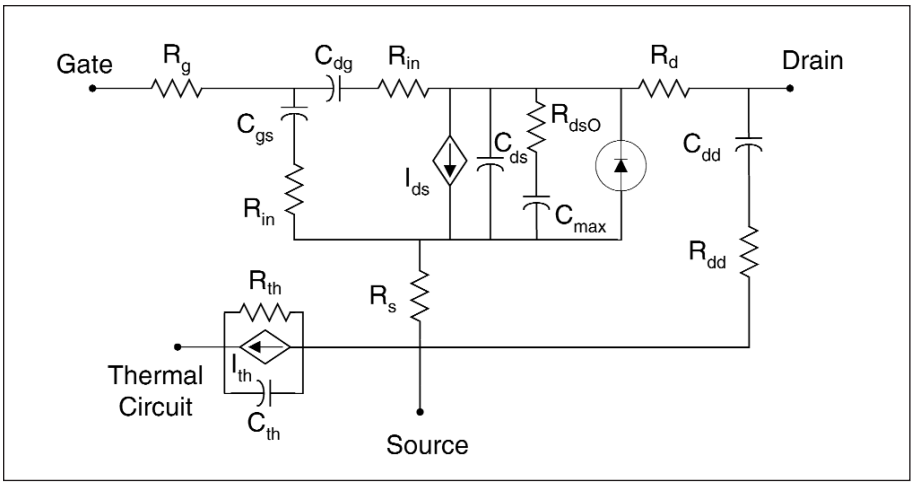

Figure 2 · Topology used in the CMC model.

baseline one watt (1 W) cell model against I-V, S-parameter, and load-pull data. Part 2, to be published in the next issue of this magazine, will demonstrate the scaling of the model and integration with package parasitics and thermal models to create a non-linear model library for an entire family of related high power transistor products. A 60 watt Doherty amplifier design example will also be presented in Part 2.

The library is now available for multiple microwave electronic design automation (EDA) software tools.

The CMC Model

The presented model is based upon the current control characteristics described by Fager, Pedro, de Carvelho and Zirath [1]. The key advantage of the Fager-Pedro model is proper treatment of current in the four regions identified in Figure 1. Shown is the measured I-V behavior of a 1 watt cell device used in this work. Most LDMOS models, including MET [2] and Yang et al. [3], implement a gate current-control characteristic that transitions from the subthreshold region to the linear gate control region directly, without treating the intermediate region, called the quadratic region. Fager et al. have implemented an equation and new parameters to fit the quadratic region. This leads to better agreement with measured IMD and other nonlinear characteristics.

The CMC (Curtice/Modelithics/Cree) model uses the current treatment of [1]. Gate charge is partitioned into gate-source and gate-drain charge. Each charge expression is a function of both V_{DS} and V_{GS}. Using charge partitioning, it is possible to fit most LDMOS capacitance functions and observed charge conservation.

The topology of the CMC model is shown in Figure 2. The CMC model includes new capacitance functions as well as modeling of the drain-source breakdown and self heating.

Self heating is treated with a special circuit as shown in Figure 2. The model has four ports, with the extra port providing a measure of the temperature rise. The voltage between the external thermal circuit port and the source node in Figure 2 is numerically equal to the junction temperature rise in degrees C. This occurs because the current source in the thermal circuit is numerically equal to the instantaneous power dissipated in the FET and the resistance, R_TH is numerically equal to the thermal resistance. The RC product of the thermal circuit is the thermal time constant.

The model also includes a silicon substrate loss circuit, consisting of a series combination of R_{dd} and C_{dd} between the external drain and source terminals. Fiorenza and del Alamo [3] have shown this effect to be significant in LDMOS power devices. The CMC model properly accommodates the observed change in pinch-off voltage with temperature as well as breakdown effects. The resulting model addresses the sharp turn-on knee in LDMOS FETs leading to the accurate prediction of double IMD sweet spots in Class AB Operation. It is also wideband, scales well, up to at least 30:1, predicts IMDs well with high dynamic range, and predicts correct performance even in Class B and C.

The code for the model has been implemented to support multiple simulators, including Agilent's Advanced Design System (ADS), and Applied Wave Research's Microwave Office, with others planned, including Eagle-ware's HARBEC and Ansoft Designer.

Model Extraction

Efficient and systematic extraction procedures have been developed and implemented in Agilent Technologies IC-CAP software. The model parameters for CMC are extracted from I-V and S-parameter data using custom routines implemented in IC-CAP. The model includes an AREA parameter for relative scaling to other size devices as compared to the original size extracted.

In the example shown in this paper, a Keithley 4200 was used for DC parametric testing and an Anritsu Lightning vector network analyzer was used for S-parameter measurements. Thermal resistance was determined using pulsed I-V measurements made over temperature using an Accent Optical Technologies Dynamic i(V) Analyzer (DiVA) D225 along with a Cascade Summit 12000 Probe Station and Microchamber. Relevant techniques are outlined and validated against

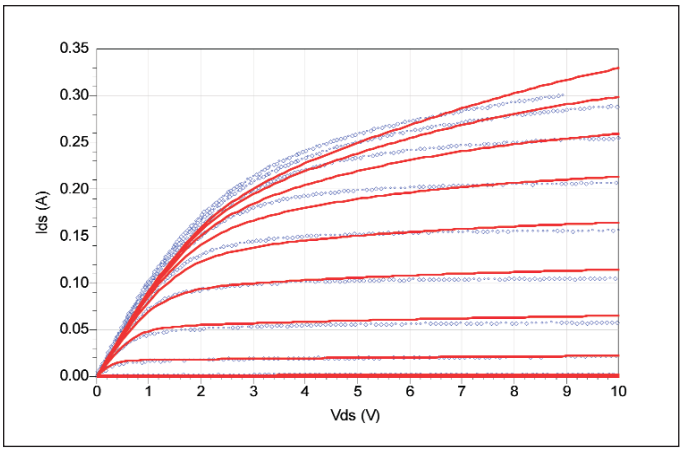

Figure 3 · Comparison of pulsed I-V data from a zero voltage quiescent condition to simulated I-V results with self heating turned off.

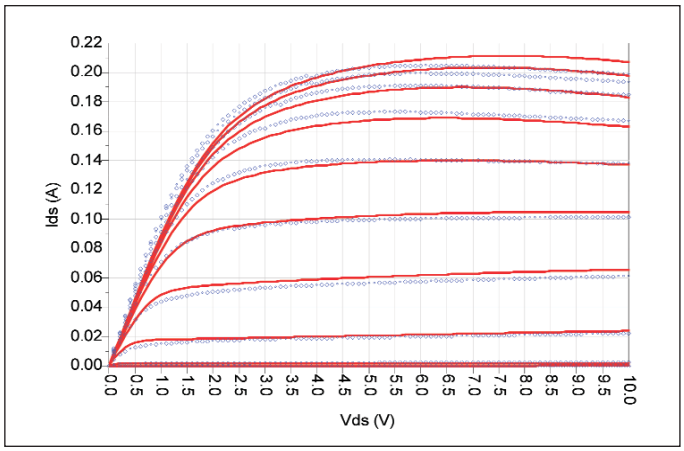

Figure 4 · Forward DC I-V curves for the 1 watt LDMOS cell showing proper treatment of self-heating effects.

the infrared thermal imaging results in [4]. This imaging system was used for the thermal resistance values used in the larger devices of the transistor library to be described in Part 2 of this paper, which will appear next month.

Current-Voltage Characteristics

Figure 3 shows a comparison of pulsed I-V data to an iso-thermal simulation made after extraction of the model parameters in IC-CAP. For this simulation the self-heating is turned off to emulate the iso-thermal measurement condition represented by the pulsed I-V data.

Figure 4 shows the average DC I-V (static) data for a one watt device as extracted in IC-CAP, and also shows the model's I-V characteristic for this device. In all figures, the solid, red line is the simulation and the blue symbols represent the data. Heating effects significantly limit the high current values. Figure 3 and 4 together demonstrate the proper functioning of the self-heating model.

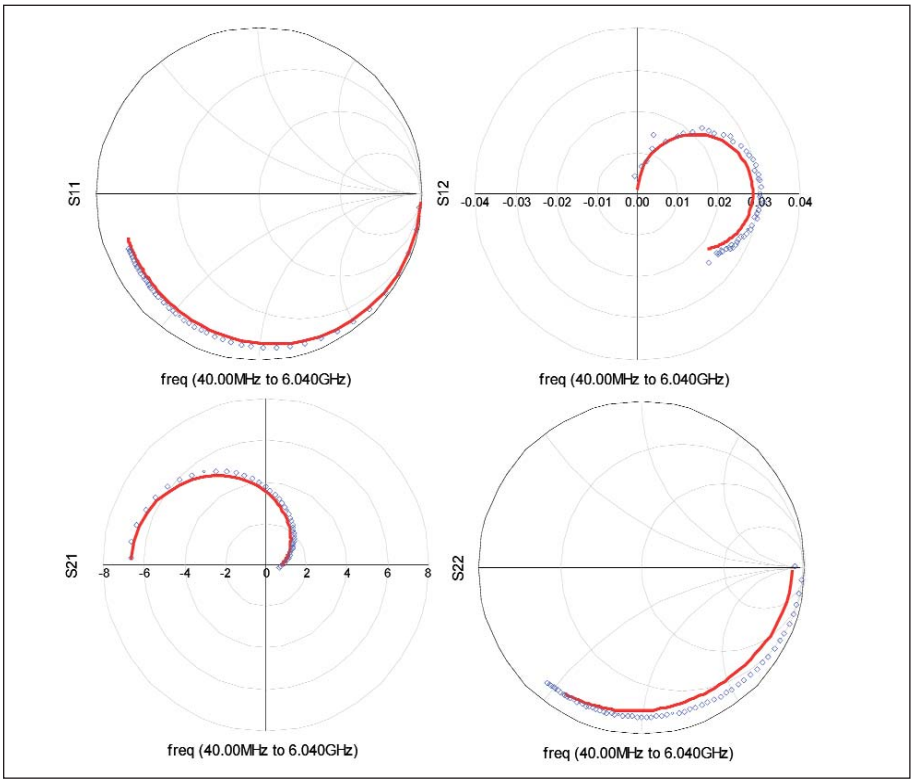

Figure 5 · Small-signal simulation for the 1 watt LDMOS cell. Displayed is measured S-parameter data (Blue circles) and an Agilent ADS simulation of the CMC model (Red line) at V_{gs} = 4.8 V and V_{ds} = 25 V.

Small-Signal Simulations

Not shown in Figure 2 are the external pad capacitances and lead inductances which are used in addition to better fit measured S-parameter data, after extraction of the intrinsic model elements and bias-dependent capacitance functions. This is done by using the developed ICCAP routine to manipulate S-parameter data taken at many bias conditions. Figure 5 shows good agreement with small-signal S-parameter simulations made using the CMC model and the small-signal measured data. Note in particular the good fits for S_{22} and S_{21} that are sometimes compromised in non-linear FET models, since the dominant parameters (g_m and R_{ds}) are derived essentially from the I-V equations.

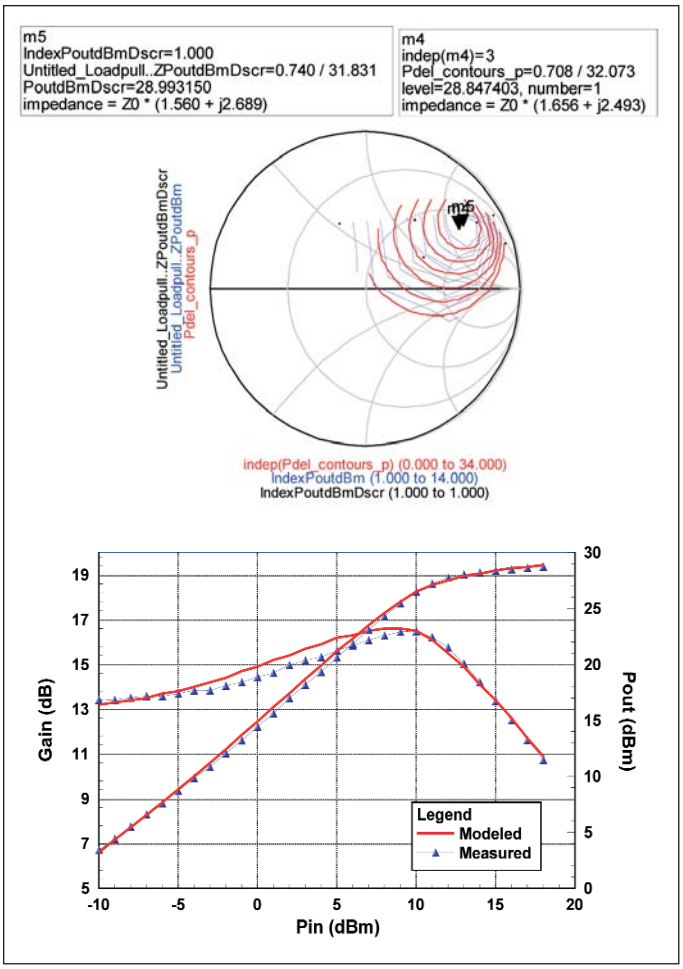

Figure 6 · Single-tone 900 MHz load pull contours are shown in the upper graph. (Blue is measured and Red is simulated data.) The lower graph shows measured and modeled power sweep data for the matching conditions determined from the load-pull simulation.

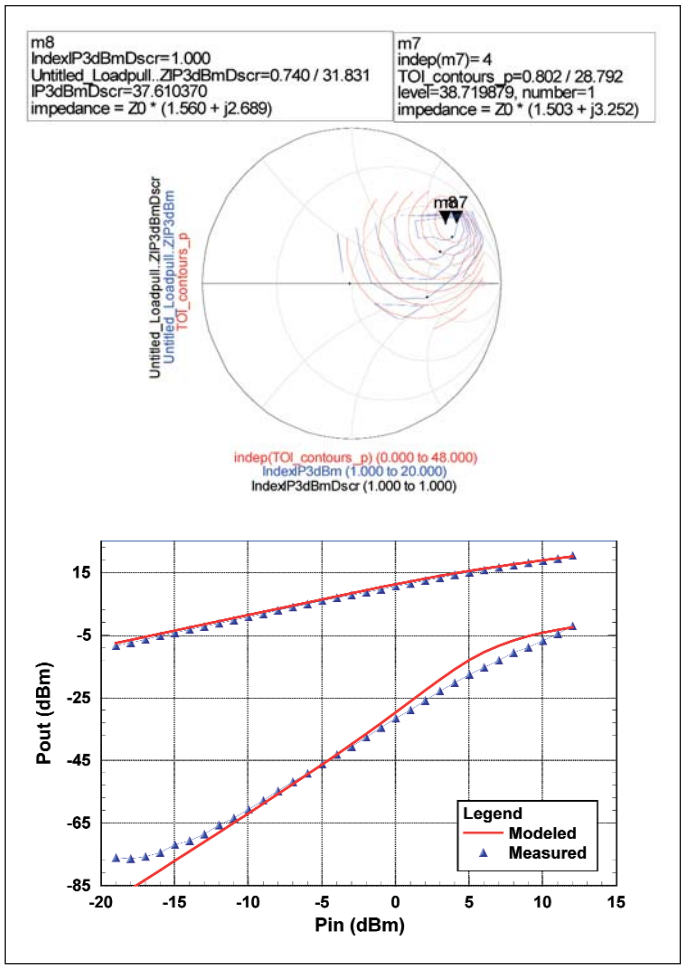

Figure 7 · Displayed are measured IP3 load-pull contours (Blue contours) and the CMC model IP3 results (Red contours) for the 1W LDMOS chip at V_{ds} = 27 V and V_{gs} = 4.8 V with input power (P_{in}) is set to 0 dBm at 900 and 910 MHz. The lower graph shows a 2-tone power sweep with the load condition held fixed at the value determined to be optimal from the load-pull simulation.

Single Tone Large-Signal Simulations

Figure 6 shows a 900 MHz load-pull simulation for the 1 watt cell performed to arrive at appropriate matching impedances to use for a power sweep. The simulation is compared to load-pull data acquired using a Maury Microwave ATS load-pull system. Figure 6 also demonstrates simulated and measured tracking for a power sweep at 900 MHz operation using the load and source impedances derived from the load-pull simulations. The simulation results shown are in good agreement with measurements. The load contours show a power of 29 dBm was reached, with close agreement on the optimal impedance near 50 × (1.6 +*j*2.6), or 80 +*j*130 ohms.

Two Tone Large-Signal Simulations

Figure 7 shows excellent simulated to modeled agreement obtained with two-tone load-pull measurements that show about a 38 dBm OIP3 level. Two-tone power sweeps also displayed in Figure 7 demonstrate good tracking of IM3 with changing power.

Conclusions

This first part of a two-part article has introduced the CMC LDMOS model that was derived to provide comprehensive treatment of LDMOS I-V behavior in the four regions of sub-threshold, quadratic, linear and compression, while also accounting for self-heating, breakdown, non-linear capacitance and careful parasitic modeling. Measured to modeled comparisons have validated the model's

IV, small-signal and non-linear simulation accuracy for a 1 watt LDMOS chip. Part 2 will be presented next month, covering application of the model for a 30-watt transistor, which is used in the design example of a 60-watt Doherty amplifier.

Acknowledgements

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Additonal information on LDMOS FET devices and the availability of the models described in this article can be obtained from either of these companies:

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